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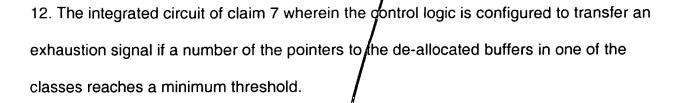
An integrated circuit that processes communication dackets, the integrated circuit comprising:

a pointer cache configured to store pointers that correspond to external buffers that are external to the integrated circuit and configured to store the communication packets; and

control logic configured to allocate the external buffers as the corresponding pointers are read from the pointer cache and de-allocate the external buffers as the corresponding pointers are written back to the pointer cache.

- 2. The integrated circuit of claim 1 wherein the control logic is configured to track a number of the pointers to the de-allocated external buffers.
- 3. The integrated circuit of claim 1 wherein the control logic is configured to transfer additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reaches a minimum threshold.
- excess portion of the pointers from the pointer cache if the number of the pointers to the de-allocated buffers reaches a maximum threshold.
- 5. The integrated circuit of claim 1 wherein the control logic is configured to transfer an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold.

- 6. The integrated circuit of claim 1 wherein the external buffers are distributed among at least two pools.
- 7. The integrated circuit of claim 1 wherein the external buffers and the pointers to the external buffers are distributed among a plurality of classes.
- 8. The integrated circuit of claim 7 wherein the control logic is configured to track a number of the pointers to the de-allocated external buffers for at least one of the classes
- 9. The integrated circuit of claim 7 wherein the control logic is configured to track a number of the pointers to the allocated external buffers for at least one of the classes
- 10. The integrated circuit of claim 7 wherein the control logic is configured to borrow at least some of the pointers from a first one of the classes for use by a second one of the classes.
- 11. The integrated circuit of claim 7 wherein the control logic is configured to redistribute at least some of the pointers from a first one of the classes to a second one of the classes.



- 13. The integrated circuit of claim 7 wherein the control logic is configured to track a number of pointers distributed to one of the classes.
- 14. The integrated circuit of claim 7 wherein at least one of the classes is associated only with constant bit rate packets.
- 15. The integrated circuit of claim 7 wherein at least one of the classes is associated only with available bit rate packets.
- 16. The integrated circuit of claim 7 wherein at least one of the classes is associated only with variable bit rate packets.
- 17. The integrated circuit of claim 7 wherein at least one of the classes is associated only with unspecified bit rate packets.

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18. A method of operating an integrated circuit that processes communication packets, the method comprising:

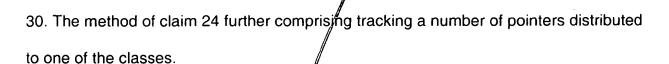
storing pointers in a pointer cache in the integrated circuit wherein the pointers correspond to external buffers that are external to the integrated circuit and that are configured to store the communication packets; and

allocating the external buffers as the corresponding pointers are read from the pointer cache; and

de-allocating the external buffers as the corresponding pointers are written back to the pointer cache.

- 19. The method of claim 18 further comprising tracking a number of the pointers to the de-allocated external buffers.
- 20. The method of claim 18 further comprising transferring additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reaches a minimum threshold.
- 21. The method of claim 18 further comprising transferring an excess portion of the pointers from the pointer cache if the number of the pointers to the de-allocated buffers reaches a maximum threshold.
- 22. The method of claim 18 further comprising transferring an exhaustion signal if a number of the pointers to the de-allocated buffers reaches a minimum threshold.

- 23. The method of claim 18 wherein the external buffers are distributed among at least two pools.
- 24. The method of claim 18 wherein the external buffers and the pointers to the external buffers are distributed among a plurality of classes.
 - 25. The method of claim 24 further comprising tracking a number of the pointers to the de-allocated external buffers for at least one of the classes
 - 26. The method of claim 24 further comprising tracking a number of the pointers to the allocated external buffers for at least one of the classes
 - 27. The method of claim 24 further comprising borrowing at least some of the pointers from a first one of the classes for use by a second one of the classes.
 - 28. The method of claim 24 further comprising re-distributing at least some of the pointers from a first one of the classes to a second one of the classes.
- 29. The method of claim 24 further comprising transferring an exhaustion signal if a number of the pointers to the de-allocated buffers in one of the classes reaches a minimum threshold.



- 31. The method of claim 24 wherein at least one of the classes is associated only with constant bit rate packets.
- 32. The method of claim 24 wherein at least one of the classes is associated only with available bit rate packets.
- 33. The method of claim 24 wherein at least one of the classes is associated only with variable bit rate packets.
- 34. The method of claim 24 wherein at least one of the classes is associated only with unspecified bit rate packets.